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(54) Name of Invention: Method of Fabricating Semiconductor Device

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Specifications

1. **Name of Invention:** Method of Fabricating Semiconductor Device

2. **Scope of Patent Application:** A method of fabricating semiconductor devices which is characterized by using a process that forms thin organic silicon films on semiconductor substrates and a process that removes the thin organic silicon film's organic functional group from the surface to a prescribed depth so as to form a dual-layered structure of silicon oxide film and thin organic silicon film on the semiconductor substrate.

3. **Detailed Explanation of Invention**

Field for Commercial Utilization: This invention relates to a method for fabricating highly reliable semiconductor devices having a multilayer wiring structure.

Existing Technology: In order to get highly reliable multilayer wiring structures in semiconductor devices it is necessary to flatten the films between the metallic wiring layers. For the usual flattening, etch-back methods and lift-off methods are used. These methods are premised on interlayer films completely embedding the spaces between the metallic wiring. However, in recent years, with the high integration of semiconductor devices, these spaces between metallic wiring have become small, making it difficult to embed dielectric films. So, it has become difficult to do the flattening by the above methods.

Of late, a bias-sputter method has been found that can embed dielectric film even in narrow spaces between the metallic wiring; but bias sputtering has the shortcoming of damaging elements formed on the substrate. So, what has been drawing attention is a method called spin-on glass. In this, a solution containing organic or inorganic silicon is applied to the substrate and heat is applied to form a thin organic or inorganic film to make it possible to embed and flatten even narrow spaces between the metallic wiring by forming dielectric film with liquid applications. Yet, the spin-on glass method has a defect: cracks or peeling easily occurring in the silicon oxide film that the spin-on glass method creates, meaning that insulating properties of thin organic silicon films formed this way are inadequate.

Problems the Invention Seeks to Resolve: To get semiconductor devices with a highly reliable multilayered wiring structure, the film between metallic wiring layers must be flattened. But, as discussed above, now with the advance in element miniaturization, present methods of flattening have reached their limit. So, we inventors have considered the shortcomings in the existing methods and looked into a spin-on glass method that could cope, even as miniaturiz-ation of elements proceeds. Thus, we came to complete this invention as a result of studies and research on methods that would do flattening by using the spin-on glass method but combine the strengths of both silicon oxide film and thin organic silicon film with a method that would not generate cracks or flaking off even when the insulativity is made high.

Means to Resolve Problems: Change to a dual-layer strúcture--a silicon oxide film layer and a thin organic

silicon film layer--by applying a solution containing organic silicon to a semiconductor substrate having an irregular surface, doing heat processing and then exposing the substrate to an oxygen plasma to remove the thin organic silicon film surface's organic functional group.

Effects: When, after making the thin organic silicon film, one exposes it to an oxygen plasma to create a dual-layered structure of silicon oxide film and thin organic silicon film, the presence of thin organic silicon film below makes it difficult for cracking or peeling to occur. Also, since it is silicon oxide film that is in contact with the overlying metallic wiring, the insulating properties are sufficient. Semiconductor devices are thus yielded that have a multi-layered wiring structure of high reliability.

Application Example: Below, we will explain this invention in detail, based on the figures.

Figures 1 to 4 are enlarged partial cross sections showing the processes of one application example of a semiconductor device from this invention.

In Figure 1, after forming field oxide film 2 by using the selective oxidation method on semiconductor substrate 1, one successively forms gate oxide film 2 and polysilicon gate 4 and uses ion-injection to install dispersion layer 5 in the source/drain area. Next, one forms 1st interlayer dielectric film 6 of phosphor-boron glass or the like, and makes contact hole 7 by anisotropic etching. On top of this is formed 1-μ thick aluminum wiring 8 and then 2nd interlayer dielectric film 9 of about 5000Å. For 2nd interlayer dielectric film 9 a silicon oxide film or the like made by plasma CVD is suitable. Then one applies about 3000Å of a solution containing organic silicon. For this one uses a solution with a chemical having a structure of $(C_6H_5)_nSi(OH)_{4-n}$. As the liquid containing organic silicon is inserted into narrow grooves, irregularities present before the application can be mostly eliminated.

Next one does heat processing of semiconductor substrate 1 (raising the temperature in several stages from room temperature, ending at 450°C after 30 minutes) to form thin organic silicon film 10 (Fig. 2). After that, one exposes semiconductor substrate 1 to an oxygen plasma for 10 minutes to remove thin organic silicon film 10's organic functional group to a prescribed depth, converting it to a silicon oxide film. That makes most of the thin parts of the thin organic silicon film formed initially into silicon oxide

film so that only the thick film areas remain as thin organic silicon film 10 in a dual-layer structure with silicon oxide film 11 (Figure 3). Through hole 12 is opened between the wiring layers on the substrate and 2nd aluminum wiring 13 is formed (Fig. 4). Because the organic silicon liquid was applied onto the substrate to flatten it, 2nd aluminum wiring 13 will not easily get broken wires or shorts. Moreover, since it is silicon oxide film 11 that is in direct contact with 2nd aluminum wiring 13, the insulating traits are sufficient. Again, the thick places between 1st aluminum wiring 8 and 2nd aluminum wiring 13 have the dual-layer structure of silicon oxide film and thin organic silicon film and since the thin organic silicon film is the lower layer, cracks will not easily intrude.

It is desirable that the solution containing organic silicon used in this invention's fabricating method include compounds having the structure of $RnSi(OH)_{4-n}$ (R: alkyl base) or $Si(OR)_4$ (R: alkyl base). Of these the $(C_6H_5)_nSi(OH)_{4-n}$ solution used in this application example showed very superior properties.

Invention's Effectiveness: If one uses the fabricating method of this invention, one can flatten interlayer films between metallic wiring layers by simple processes. Also, since silicon oxide film and thin organic silicon film are combined, one can get semiconductor devices which have good insulativity, which scarcely gets cracks or peeling and whose reliability is high.

Because flattening is done by a liquid application, the fabricating method of this invention can cope even with further advances hereafter in element miniaturization. Such a fabrication method has a very high commercial value not seen elsewhere.

4. Simple Explanation of Figures

Figures 1 through 4 show the processes of one application example when fabricating a semiconductor device with this invention. Figure 1 is an enlarged partial cross section of a semiconductor device using the fabricating method from this invention. Figure 2 is an enlarged partial cross section of a semiconductor substrate after the thin organic silicon film is formed. Figure 3 is an enlarged partial cross section of a semiconductor substrate after exposure to

oxygen plasma. Figure 4 is an enlarged partial cross section after 2nd aluminum wiring is formed using the fabrication method of this invention.

1 … Semiconductor substrate
2 … Field oxide film
3 … Gate oxide film
4 … Polysilicon gate
5 … Dispersion layer
6 … 1st interlayer dielectric film
7 … Contact hole
8 … 1st aluminum wiring
9 … 2nd interlayer dielectric film
10 … Thin organic silicon film
11 … Silicon oxide film
12 … Through hole
13 … 2nd aluminum wiring

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